WHAT IS CLAIMED IS:

1. A liquid crystal display device having an interconnection line part for applying a signal from a driving circuit to a liquid crystal display comprising:

a substrate; and

a plurality of interconnection lines on the substrate, the interconnection lines are wider at a center portion of the interconnection line part than at an outer portion of the interconnection line part.

2. The liquid crystal display device as claimed in claim 1, wherein each respective interconnection line includes a first straight-line part to which the driving IC is connected; a second straight-line part connected to gate lines or data lines of an LCD panel; and a slanted part for connecting the first straight-line part with the second straight-line part.

3. The liquid crystal display device as claimed in claim 2, wherein the respective interconnection lines are thickly formed in only the first and second straight-line parts.

4. A liquid crystal display device comprising:

a plurality of interconnection lines for applying a signal from a driving circuit to a liquid crystal display panel; and

a plurality of supplementary conductive patterns between the interconnection lines and connected with respective ones of interconnection lines.

5. The liquid crystal display device as claimed in claim 4, wherein the supplementary conductive patterns are of the same materials as gate lines or data lines of the liquid crystal display panel.

6. The liquid crystal display device as claimed in claim 4, wherein the interconnection lines are in an interconnection line region having a center portion and an outer portion and wherein the supplementary conductive patterns connected to the interconnection lines in the center portion have a larger area than the supplementary conductive patterns connected to the interconnection lines in the outer portion.

7. A liquid crystal display device having an interconnection line part for applying a signal from a driving circuit to a liquid crystal display panel, comprising:

a substrate;

a conductive layer formed on the substrate of the interconnection line part, the conductive layer being wider in a center portion of the interconnection line part rather than in an outer portion of the interconnection line part;

an insulating film on the entire substrate including the conductive layer; and

a plurality of interconnection lines arranged to overlap the conductive layer on the insulating film.

8. The liquid crystal display device as claimed in claim 7, wherein a plurality of capacitors are formed between the plurality of interconnection lines and the conductive layer, and capacitance of the capacitors between a respective interconnection line and the conductive layer is greater at the center portion than at the outer portion.

9. The liquid crystal display device as claimed in claim 8, wherein the capacitances of the capacitors between the respective interconnection lines and the conductive layer gradually increases from the outer portion to the center portion.

10. The liquid crystal display device as claimed in claim 7, wherein a voltage for preventing static electricity is applied to the conductive layer.

11. The liquid crystal display device as claimed in claim 7, wherein a common voltage is applied to the conductive layer.

12. The liquid crystal display device as claimed in claim 7, wherein the conductive layer is formed of a semiconductor layer doped with impurities.

13. The liquid crystal display device as claimed in claim 7, wherein the conductive layer is formed in a roughly triangle shape, so that the conductive layer overlapped with the interconnection line at an outer portion of the interconnection line part has a smaller area than at a center portion of the interconnection line part.

14. The liquid crystal display device as claimed in claim 7, wherein the insulating film has a double structure of a gate insulating film and an interlayer insulating film.

15. The liquid crystal display device as claimed in claim 7, further comprising a plurality of supplementary lines between the interconnection lines and electrically connected with respective interconnection lines.

16. The liquid crystal display device as claimed in claim 15, wherein the plurality of supplementary lines are formed of the same materials as the interconnection lines.

17. The liquid crystal display device as claimed in claim 15, wherein the plurality of supplementary lines are formed with the same size as one another.

18. The liquid crystal display device as claimed in claim 7, wherein the interconnection lines are data interconnection lines.

19. The liquid crystal display device as claimed in claim 7, wherein the conductive layer is formed of the same material as a gate line of the liquid crystal display panel.

20. A liquid crystal display device having an interconnection line part for applying a signal from a driving circuit to a liquid crystal display panel, comprising:

a substrate;

a plurality of interconnection lines arranged on the substrate;

an insulating film formed on the entire surface of the substrate including the plurality of interconnection lines; and

a conductive layer formed on the substrate of the interconnection lines, the conductive layer having a larger area in a center portion of the interconnection line part than in an outer portion of the interconnection line part.

21. The liquid crystal display device as claimed in claim 20, wherein a voltage for preventing static electricity is applied to the conductive layer.

22. The liquid crystal display device as claimed in claim 20, wherein a common voltage is applied to the conductive layer.

23. The liquid crystal display device as claimed in claim 20, wherein the interconnection lines are gate interconnection lines, and the conductive layer is formed of the same material as that of a data line of the liquid crystal display panel.

24. The liquid crystal display device as claimed in claim 20 further comprising a plurality of supplementary lines electrically connected to respective interconnection lines.

25. A method for fabricating a liquid crystal display device having a data interconnection line part for applying a signal from a driving circuit to a liquid crystal display panel; and a cell array part in which a plurality of gate lines cross a plurality of data lines to define a pixel region, and thin film transistors (TFTs) are formed at the crossing of the gate and data lines, comprising:

forming a first active layer in an island shape in the region where the respective TFTs of the cell array part are formed, and forming a second active layer on the substrate;

forming a gate insulating film on the entire surface including the first and second active layers;

forming a plurality of gate lines having gate electrodes extending therefrom on the first active layer;

forming source and drain regions in the first active layer by impurity ion implantation using the gate electrodes as a mask, and forming a conductive layer in the second active layer;

forming an interlayer insulating film on the entire surface of the source and drain regions to form a contact hole; and

forming a plurality of data lines and data interconnection lines, the data lines connected to the source and drain regions and formed substantially perpendicular to the gate lines, so that the data interconnection line part has a wider area in a center portion of the data interconnection line part than in an outer portion of the data interconnection line part and a capacitance of the data interconnection lines with the second active layer is gradually increased towards the center portion from the outer portion.

26. The method as claimed in claim 25 further comprising forming a plurality of supplementary lines of the same material as that of the data interconnection lines so as to be electrically connected to the respective data interconnection lines.

27. A method for fabricating a liquid crystal display device having a data interconnection line part for applying a signal from a driving circuit to a liquid crystal display panel; and a cell array part in which a plurality of gate lines cross a plurality of data lines to define a pixel region, and thin film transistors (TFTs) are formed at the crossing of the gate and data lines, comprising:

forming a plurality of gate lines having gate electrodes in the region where the TFTs are formed and simultaneously forming a gate metal pattern layer having a wider area in a center portion of the data interconnection line part than in an outer portion of the data interconnection line part;

forming a gate insulating film on the entire surface including the gate line and the gate metal pattern layer;

forming an active layer in an island shape in the region where the respective TFTs are formed; and

forming a plurality of data lines and data interconnection lines substantially perpendicular to the gate lines, so that source and drain electrodes are formed on both sides of the active layer, and a capacitance between the data interconnection lines and the gate metal pattern layer is gradually increased towards the center portion of the data interconnection line part from the outer portion of the data interconnection line part.

28. The method as claimed in claim 27, further comprising forming a plurality of supplementary lines of the same material as the data interconnection lines so as to be electrically connected to respective data interconnection lines.

29. A method for fabricating a liquid crystal display device having a data interconnection line part for applying a signal from a driving circuit to a liquid crystal display panel; and a cell array part in which a plurality of gate lines cross a plurality of data lines to define a pixel region, and thin film transistors (TFTs) having source and drain electrodes are formed at the crossing of the gate and data lines, comprising:

forming an active layer in the region where the TFTs are formed;

forming a gate insulating film on the entire surface of the substrate;

forming a plurality of gate lines on the gate insulating film at the cell array part and forming a gate metal pattern layer on the gate insulating film at the data interconnection line part, so that a gate electrode is formed above the active layer, and so that the gate metal pattern is wider at a center portion of the data interconnection line part than an outer portion of the data interconnection line part;

forming an impurity region in the active layer using the gate electrode as a mask, and forming an interlayer insulating film on the entire surface including the gate line and the gate metal pattern layer so as to form a contact hole in the impurity region; and

forming a plurality of data and data interconnection lines substantially perpendicular to the gate lines, so that source and drain electrodes are connected to the impurity region through the contact hole, and a capacitance with the gate metal pattern layer is gradually increased towards the center portion from the outer portion.

30. The method as claimed in claim 29, further comprising forming a plurality of supplementary lines of the same material as the data interconnection lines so as to be electrically connected to respective data interconnection lines.

31. A method for fabricating a liquid crystal display device having a gate interconnection line part for applying a signal from a driving circuit to a liquid crystal display panel; and a cell array part in which a plurality of gate lines cross a plurality of data lines to define a pixel region, and thin film transistors (TFTs) are formed at the crossing of the gate and data lines, comprising:

forming an active layer in the region where the TFTs are formed;

forming a gate insulating film on the entire surface of the active layer;

forming a plurality of gate lines and gate interconnection lines on the gate insulating film so as to form a gate electrode on the active layer;

forming an impurity region in the active layer using the gate electrode as a mask, and forming an interlayer insulating film on the entire surface including the gate lines and the gate interconnection lines so as to form a contact hole in the impurity region; and

forming a plurality of data lines substantially perpendicular to the gate lines to connect source and drain electrodes to the impurity region through the contact hole, and simultaneously forming a data metal pattern layer to overlap the gate interconnection lines,

so that the data metal pattern layer is wider at a center portion of the gate interconnection line part than at an outer portion of the gate interconnection line part.

32. The method as claimed in claim 31, further comprising forming a plurality of supplementary lines of the same material the gate interconnection lines so as to be electrically connected to respective gate interconnection lines.

33. A method for fabricating a liquid crystal display device having a gate interconnection line part for applying a signal from a driving circuit to a liquid crystal display panel; and a cell array part in which a plurality of gate lines cross a plurality of data lines to define a pixel region, and thin film transistors (TFTs) are formed at the crossing of the gate and data lines, comprising:

forming a plurality of gate lines and gate interconnection lines having gate electrodes in the region where the TFTs are formed;

forming a gate insulating film on the entire surface including the gate lines and the gate interconnection lines;

forming an active layer in an island shape in the region where the TFTs are formed; and

forming a plurality of data lines substantially perpendicular to the gate lines to form source and drain electrodes on both sides of the active layer, and simultaneously forming a data metal pattern layer to overlap the gate interconnection lines, so that the data metal pattern layer is wider at a center portion of the gate interconnection line part than at an outer portion of the gate interconnection line part

34. The method as claimed in claim 33, further comprising forming a plurality of supplementary lines of the same material as the gate interconnection lines so as to be electrically connected to the gate interconnection lines.